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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/660,882	PREISS, FRANK	
	Examiner	Art Unit	
	Kevin Mew	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,8-10 and 12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2, 4-6, 8-10, 12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final Action

Response to Amendment

1. Applicant's remarks/arguments filed on 5/29/2007 regarding claims 1-2, 4-6, 8-10, 12-17 have been considered. Claims 1-2, 4-6, 8-10, 12-17 are currently pending. Claims 3, 7, 11 and 18 have been canceled by the Applicant.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lamb (USP 6,587,454) in view of Rabenko et al. (USP 7,023,868).

Regarding claim 1, Lamb discloses a processor for use in a Voice-over-Internet Protocol telephone (**MAC/DSP circuits**, element 73, Fig. 5), including:

a Voice-over-Internet Protocol processor core (**MAC/DSP circuits**, element 73, Fig. 5) operable to transmit computer data and voice data over a computer network (**voice packets are transmitted onto network hub**, col. 6, lines 54-61 and element 67, Fig. 5), the processor core including one or more pipelines (a pipeline connecting between MAC/DSP circuits 73 and node core logic 75, Fig. 5);

a bus (**node core logic**, element 75, Fig. 5; note that a node core logic is considered as a bus because it interconnects MAC circuits 64, 72 and MAC/DSP circuits 73 through receiving

signals from and transmitting signals to these circuits, Fig. 5) on which signals internal to the processor (**MAC/DSP circuits**, element 73, Fig. 5) are routed;

one or more communication ports (**upstream packet network port**, element 66, Fig. 5) coupled to the Voice-over-Internet Protocol processor core (**upstream packet network port 66 coupled to the core MAC/DSP circuits 73**, elements 66, 73, Fig. 5) through the bus (**through the node core logic**, element 75, Fig. 5),

a repeater (**node core logic 75 comprises a repeater**, col. 6, lines 1-24 and col. 7, lines 1-4) coupled to the Voice-over-Internet Protocol processor core (**the repeater coupled to the core MAC/DSP circuits**, element 73, Fig. 5) through the bus (**through the node core logic**, element 73, Fig. 5);

one or more IEEE 802.3 media access controllers (MACs) (**IEEE 802.x MAC circuits 64**, col. 6, lines 43-53 and element 64, Fig. 5) coupled to the Voice-over-Internet Protocol processor core (**coupled to the MAC/DSP circuits 73**, Fig. 5) through the bus (**through the node core logic**, element 75, Fig. 5), the one or more MACs being separate from the Voice-over-Internet Protocol processor core (one or more MACs 64 and 72 being separate from the Voice and Data Processor 73, Fig. 5).; and

wherein the Voice-over-Internet Protocol processor core (**MAC/DSP circuits**, element 73, Fig. 5) transmits the computer data and the voice data (**MAC/DSP circuits transmit computer and voice data**, col. 6, lines 54-61 and element 67, Fig. 5), and wherein the repeater (**the repeater**, col. 6, lines 1-24, col. 7, lines 1-4 and element 75, Fig. 5), the one or more communication ports (**upstream packet network port**, element 66, Fig. 5) and the one or more IEEE 802.3 MACs (**IEEE 802.x MAC circuits 64**, col. 6, lines 43-53 and element 64, Fig. 5)

are each integrated to the Voice-over-Internet Protocol processor core (**MAC/DSP circuits**, element 73, Fig. 5).

Lamb does not explicitly show an on-chip memory coupled to the Voice-over-Internet Protocol processor core through the bus, the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core, wherein the Voice-over-Internet Protocol processor core, the repeater, the one or more communication ports and the one or more IEEE 802.3 MACs are each integrated onto a same chip as the Voice-over-Internet Protocol processor core, and the one or more MACs being separate from the Voice-over-Internet Protocol processor core.

However, Rabenko discloses a single chip device comprising an on-chip memory (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3) coupled to a voice and data processor core (Voice and Data Processor) and the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3, col. 7, lines 41-55).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Lamb with the teaching of Rabenko in implementing VoIP processor core, data memory and program memory on a single chip such that the processor core of Lamb will comprise an on-chip memory coupled to the Voice-over-Internet Protocol processor core through the bus, the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core, and the Voice-over-Internet Protocol processor core, the repeater, the one or more communication ports

and the one or more IEEE 802.3 MACs are each integrated onto a same chip as the Voice-over-Internet Protocol processor core.

The motivation to do so is to provide a highly integrated solution implemented single chip that is compliant with the Data Over Cable Service Interface Specification (DOCSIS) such that the cable modem equipment built by a variety of manufacturers is compatible.

Regarding claim 5, Lamb discloses the processor of claim 1, wherein the one or more communication ports (**upstream packet network port**, element 66, Fig. 5) allow the Voice-over-Internet Protocol processor core to be coupled to one or more external components (**upstream packet network port allows the core MAC/DSP circuits to be coupled to telephone**, elements 71, 73, Fig. 5) without external interfacing circuitry (**without external interfacing circuitry**, Fig. 5).

3. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lamb and Rabenko, and further in view of Anandakumar et al. (USP 6,574,213)

Regarding claim 2, Lamb discloses the processor of claim 1, except fails to disclose the one or more communication ports further include one or more pulse code modulation (PCM) ports.

However, Anandakumar discloses a Voice-over-Internet Protocol network processor (DSP, see Fig. 15) that implements one or more ports in PCM (col. 24, lines 61-67).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined system of Lamb, Shnitzer, and Kramer with the

teaching of using PCM in Anandakumar such that one or more ports disclosed in Lamb is a PCM port.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lamb and Rabenko, and further in view of Shnitzer et al. (US Publication 2006/0072552).

Regarding claim 4, the combined system of Lamb and Rabenko discloses all the aspects of the claimed invention set forth in the rejection of claim 1 above, except fails to explicitly disclose that the one or more communication ports further include one or more universal serial bus (USB) ports.

However, Shnitzer discloses a system that comprises a processor subsystem and memory (**a telephone communication system**, paragraphs 0064, 0065, element 90, Fig. 5), would accept VoIP calls (paragraphs 0065, 0113, 0121-0124, 0132) and comprises a USB peripheral connect interface (**USB interface**, paragraph 0065) to provide an communication interface between the media signaling processor and digital signaling processor core (paragraph 0065 and elements 180, 170) and the USB compatible digital telephone switch controller device (element 190, Fig. 5).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Lamb with the teaching of Shnitzer in using an USB port as a communication interface between a VoIP processor core with a USB compatible device such that one or more of integrated communication ports disclosed in Lamb would be a USB port such as the coupling of VoIP processor core to USB interface, as taught by Shnitzer. The motivation to do so is to provide the capability for the VoIP processor to support

USB ports because it would allow the VoIP telephone to connect to some USB compatible peripheral devices such as digital telephone switch controller device.

5. Claims 6, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lamb and Shnitzer, and further in view of Rabenko et al.

Regarding claim 6, Lamb discloses an apparatus, comprising:

a Voice-over-Internet Protocol processor (**core MAC/DSP circuits**, element 73, Fig. 5) operable to transmit computer data and voice data over a computer network (**voice packets are transmitted onto network hub**, col. 6, lines 54-61 and element 67, Fig. 5);

a flexible peripheral interconnect bus (**node core logic**, element 75, Fig. 5);

one or more communication ports (**upstream packet network port**, element 66, Fig. 5) coupled to the Voice-over-Internet Protocol processor (**upstream packet network port 66 coupled to the core MAC/DSP circuits**, elements 66, 73, Fig. 5) through the FPI bus (**through the node core logic**, element 75, Fig. 5),

a repeater (**node core logic 75 comprises a repeater**, col. 6, lines 1-24 and col. 7, lines 1-4) coupled to the Voice-over-Internet Protocol processor core (**the repeater coupled to the core MAC/DSP circuits**, element 73, Fig. 5) through the bus (**through the node core logic**, element 75, Fig. 5); and

wherein the Voice-over-Internet Protocol processor core (**MAC/DSP circuits**, element 73, Fig. 5) transmits the computer data and the voice data (**MAC/DSP transmits computer and voice data**, col. 6, lines 54-61 and element 67, Fig. 5), and

a repeater (**a repeater**, col. 6, lines 1-24 , col. 7, lines 1-4 and element 75, Fig. 5) through the FPI bus (**through the node core logic**, element 75, Fig. 5)

one or more IEEE 802.3 MACs (IEEE 802.x MAC, col. 6, lines 17-34 and element 64, Fig. 5) are each integrated through the FPI bus (**through the node core logic**, element 75, Fig. 5).

Lamb does not explicitly disclose that the one or more communication ports are universal serial bus (USB) ports.

However, Shnitzer discloses a system that comprises a processor subsystem and memory (**a telephone communication system**, paragraphs 0064, 0065, element 90, Fig. 5), would accept VoIP calls (paragraphs 0065, 0113, 0121-0124, 0132) and comprises a USB peripheral connect interface (**USB interface**, paragraph 0065) to provide an communication interface between the media signaling processor and digital signaling processor core (paragraph 0065 and elements 180, 170) and the USB compatible digital telephone switch controller device (element 190, Fig. 5).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Lamb with the teaching of Shnitzer in using an USB port as a communication interface between a VoIP processor core with a USB compatible device such that one or more of integrated communication ports disclosed in Lamb would be a USB port such as the coupling of VoIP processor core to USB interface, as taught by Shnitzer. The motivation to do so is to provide the capability for the VoIP processor to support USB ports because it would allow the VoIP telephone to connect to some USB compatible peripheral devices such as digital telephone switch controller device.

The combined system of Lamb and Shnitzer does not explicitly show the Voice-over-Internet Protocol processor, the repeater, USB ports, and one or more IEEE MACs are integrated onto a single chip.

However, Rabenko discloses a single chip device comprising an on-chip memory (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3) coupled to a voice and data processor core (Voice and Data Processor) and the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3, col. 7, lines 41-55).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Lamb and Shnitzer with the teaching of Rabenko in implementing VoIP processor core, data memory and program memory on a single chip such that the modified processor core of Lamb and Shnitzer will comprise an on-chip memory coupled to the Voice-over-Internet Protocol processor core through the bus, the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core, and the Voice-over-Internet Protocol processor core, the repeater, the one or more communication ports and the one or more IEEE 802.3 MACs are each integrated onto a same chip as the Voice-over-Internet Protocol processor core.

The motivation to do so is to provide a highly integrated solution implemented single chip that is compliant with the Data Over Cable Service Interface Specification (DOCSIS) such that the cable modem equipment built by a variety of manufacturers is compatible.

Regarding claim 10, Lamb discloses an apparatus, comprising:

a Voice-over-Internet Protocol processor (**core MAC/DSP circuits**, element 73, Fig. 5) operable to transmit computer data and voice data over a computer network (**voice packets are transmitted onto network hub**, col. 6, lines 54-61 and element 67, Fig. 5);

a flexible peripheral interconnect bus (**node core logic**, element 75, Fig. 5);

one or more communication ports (**upstream packet network port**, element 66, Fig. 5) coupled to the Voice-over-Internet Protocol processor (**upstream packet network port 66 coupled to the core MAC/DSP circuits**, elements 66, 73, Fig. 5) through the FPI bus (**through the node core logic**, element 75, Fig. 5),

a repeater (**node core logic 75 comprises a repeater**, col. 6, lines 1-24 and col. 7, lines 1-4) coupled to the Voice-over-Internet Protocol processor core (**the repeater coupled to the core MAC/DSP circuits**, element 73, Fig. 5) through the bus (**through the node core logic**, element 75, Fig. 5); and

wherein the Voice-over-Internet Protocol processor core (**MAC/DSP circuits**, element 73, Fig. 5) transmits the computer data and the voice data (**MAC/DSP transmits computer and voice data**, col. 6, lines 54-61 and element 67, Fig. 5), and

a repeater (**a repeater**, col. 6, lines 1-24 , col. 7, lines 1-4 and element 75, Fig. 5) integrated onto the same chip (**integrated onto the same adaptor 65**, Fig. 5) through the FPI bus (**through the node core logic**, element 75, Fig. 5)

one or more IEEE 802.3 MACs (IEEE 802.x MAC, col. 6, lines 17-34 and element 64, Fig. 5) are through the FPI bus (**through the node core logic**, element 75, Fig. 5).

Lamb does not explicitly disclose that the one or more communication ports are universal serial bus (USB) ports.

However, Shnitzer discloses a system that comprises a processor subsystem and memory (**a telephone communication system**, paragraphs 0064, 0065, element 90, Fig. 5), would accept VoIP calls (paragraphs 0065, 0113, 0121-0124, 0132) and comprises a USB peripheral connect interface (**USB interface**, paragraph 0065) to provide an communication interface between the media signaling processor and digital signaling processor core (paragraph 0065 and elements 180, 170) and the USB compatible digital telephone switch controller device (element 190, Fig. 5).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Lamb with the teaching of Shnitzer in using an USB port as a communication interface between a VoIP processor core with a USB compatible device such that one or more of integrated communication ports disclosed in Lamb would be a USB port such as the coupling of VoIP processor core to USB interface, as taught by Shnitzer. The motivation to do so is to provide the capability for the VoIP processor to support USB ports because it would allow the VoIP telephone to connect to some USB compatible peripheral devices such as digital telephone switch controller device.

The combined system of Lamb and Shnitzer does not disclose the single-chip Voice-over-Internet Protocol processor comprises a memory unit coupled to the Voice-over-Internet Protocol processor, the memory unit operable to store programs used by the Voice-over-Internet Protocol network processor, and the .

However, Rabenko discloses a single chip device comprising an on-chip memory (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3) coupled to a voice and data processor core (Voice and Data Processor) and the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3, col. 7, lines 41-55).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP processor of Lamb with the teaching of Rabenko in implementing VoIP processor core, data memory and program memory on a single chip such that the processor core of Lamb will comprise an on-chip memory coupled to the Voice-over-Internet Protocol processor core through the bus, the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core, and the Voice-over-Internet Protocol processor core, the repeater, the one or more communication ports and the one or more IEEE 802.3 MACs are each integrated onto a same chip as the Voice-over-Internet Protocol processor core.

The motivation to do so is to provide a highly integrated solution implemented single chip that is compliant with the Data Over Cable Service Interface Specification (DOCSIS) such that the cable modem equipment built by a variety of manufacturers is compatible.

6. Claims 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lamb as in view of Shnitzer et al. and Rabenko et al., and in further view of Anandakumar (USP 6,574,213).

Regarding claim 8, the combined system of Lamb, Shnitzer and Rabenko discloses all the aspects of the claimed invention set forth in the rejection of claim 6 above, except fails to disclose wherein the single-chip Voice-lover-Internet Protocol network processor (the adaptor 65, Fig. 5) further includes the one or more ports are pulse code modulation (PCM) ports.

However, Anandakumar discloses a Voice-over-Internet Protocol network processor (DSP, see Fig. 15) that implements one or more ports that PCM (col. 24, lines 61-67).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined system of Lamb, Shnitzer and Rabenko with the teaching of using PCM in Anandakumar such that one or more ports disclosed in Lamb is a PCM port.

The motivation to do so is to provide voice coding functionality for voice samples in the adaptor of Lamb.

Regarding claim 9, the combined system of Lamb, Shnitzer, Rabenko and Anandakumar discloses the apparatus of claim 8, Anandakumar further discloses each PCM port is operable to handle up to 30 time slots (24 time slots, see line 34, col. 28) and wherein each time slot is capable of handling a 64K bit/sec voice channel (PCM is 64kbps, see col. 24, lines 61-67).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined system of Lamb, Shnitzer and Rabenko with the teaching of using PCM in Anandakumar such that one or more ports disclosed in Lamb is a PCM port.

The motivation to do so is to provide voice coding functionality for voice samples in the adaptor of Lamb such that it conforms with the G.711 PCM voice coding standard.

7. Claims 12-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lamb in view of Shnitzer et al. (US Patent 6,526,131) and Rabenko et al., and in further view of Anandakumar (USP 6,574,213).

Regarding claim 12, the combined system of Lamb, Shnitzer and Rabenko discloses the system of claim 10, except fails to disclose the port is a PCM port.

However, Anandakumar discloses a Voice-over-Internet Protocol network processor (DSP, see Fig. 15) that implements one or more ports in PCM (col. 24, lines 61-67).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined system of Lamb, Shnitzer and Rabenko with the teaching of using PCM in Anandakumar such that one or more ports disclosed in Lamb is a PCM port.

The motivation to do so is to provide voice coding functionality for voice samples in the adaptor of Lamb.

Regarding claim 13, the combined system of Lamb, Shnitzer, Rabenko and Anandakumar discloses the system of claim 12. Anandakumar further discloses each PCM port is operable to handle up to 30 time slots (24 time slots, see line 34, col. 28) and wherein each time slot is capable of handling a 64K bit/sec voice channel (PCM is 64kbps, see col. 24, lines 61-67).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the combined system of Lamb, Shnitzer, and Rabenko with the teaching of using PCM in Anandakumar such that one or more ports disclosed in Lamb is a PCM port.

The motivation to do so is to provide voice coding functionality for voice samples in the adaptor of Lamb such that it conforms with the G.711 PCM voice coding standard.

Regarding claim 14, the combined system of Lamb, Shnitzer, Rabenko and Anandakumar discloses the system of claim 12. Lamb further comprising a digital-to-analog/analog-to-digital (DA/AD) converter connected to the single-chip Voice-over-Internet Protocol network processor (MAC/DSP circuits perform AD/DA conversion, element 73, Fig. 5).

Regarding claim 15, the combined system of Lamb, Shnitzer, Rabenko and Anandakumar discloses the system of claim 14. Lamb further discloses comprising a microphone (telephone, element 10, Fig. 2), a speaker (element 10, Fig. 2), and a handset (see element 10, Fig. 2), each connected to the single-chip Voice-over-Internet Protocol network processor through the DA/AD converter (telephone 10 coupled to the MAC/DSP circuits, element 73, Fig. 5).

Regarding claim 16, the combined system of Lamb, Shnitzer, Rabenko and Anandakumar discloses the system of claim 15. Lamb further discloses the system of claim 15, further comprising a keypad interfaced with the single-chip Voice-over-Internet Protocol network

processor, the keypad operable to allow a user to dial telephone numbers (telephone, element 10, Fig. 2).

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lamb in view of Shnitzer et al. (US Patent 6,526,131), Rabenko et al., Anandakumar (USP 6,574,213), and in further view of Edholm (USP 6,449,269).

Regarding claim 17, the combined system of Lamb, Shnitzer, Rabenko and Anandakumar discloses all the aspects of the claimed invention set forth in the rejection of claim 16 above, except fails to explicitly disclose the system of claim 16, further comprising a liquid crystal display (LCD) operable to display information entered through the keypad.

However, Edholm discloses a connectivity box (a system) that comprises of a VoIP telephone (lines 27-30, col. 4 and element 100, Fig. 2) with a LCD display operable to display the digits keyed in via keypad of the IP telephone (lines 36-52, col. 5, element 260, Fig. 2).

Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify the VoIP system of Lamb with the VoIP telephone of Edholm such that a LCD display is interfaced with the VoIP processor of the VoIP telephone to display information entered through the keypad such as LCD display of the VoIP telephone taught by Edholm. The motivation to do so is to provide inexpensive output screen on the IP telephone to display user feedback regarding the digits keyed in via keypad of the IP telephone and/or status of the phone itself because it reduces the development and manufacturing costs of the IP phone.

Response to Arguments

9. Applicant's arguments filed on /29/2007 with respect to claims 1, 6 and 8-10 have been considered but they are not persuasive.

Applicant argued on page 1, last paragraph and page 2, first paragraph of the Remarks that neither Lamb nor Rebenko teaches or suggests "one or more MACs being separate from the Voice-over-Internet processor core," the examiner respectfully disagrees. It is recognized by the examiner that Lamb discloses one or more 802.3 Ethernet MAC (elements 64, 72, Fig. 5) is separate from the Voice and Data Processor (element 73, Fig. 5).

In response to applicant's arguments on page 2, paragraphs 3-4 of the Remarks that the combination of Lamb and Rabenko does not teach or suggest "a repeater, one or more communication ports, and one or more IEEE 802.3 MACs that are each integrated onto a same chip as a Voice-over-Internet Protocol processor core," the examiner respectfully disagrees.

As shown in the rejection of claim 1 above, it is noted that Lamb discloses one or more communication ports (**upstream packet network port**, element 66, Fig. 5) coupled to the Voice-over-Internet Protocol processor core (**upstream packet network port 66 coupled to the core MAC/DSP circuits 73**, elements 66, 73, Fig. 5) through the bus (**through the node core logic**, element 75, Fig. 5), a repeater (**node core logic 75 comprises a repeater**, col. 6, lines 1-24 and col. 7, lines 1-4) coupled to the Voice-over-Internet Protocol processor core (**the repeater coupled to the core MAC/DSP circuits**, element 73, Fig. 5) through the bus (**through the node core logic**, element 73, Fig. 5); one or more IEEE 802.3 media access controllers (MACs) (**IEEE 802.x MAC circuits 64**, col. 6, lines 43-53 and element 64, Fig. 5) coupled to

the Voice-over-Internet Protocol processor core (**coupled to the MAC/DSP circuits 73**, Fig. 5) through the bus (**through the node core logic**, element 75, Fig. 5).

Lamb may not explicitly show these components are each integrated onto s same chip. However, Rabenko cures these deficiencies by teaching a single chip device comprising an on-chip memory (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3) coupled to a voice and data processor core (Voice and Data Processor, element 160, Fig. 3), 802.3 Ethernet MAC (element 134, Fig. 3) coupled to the voice and data processor core 160, and the on-chip memory including a program memory to include instruction and a data memory to store cache for the processor core (an on-chip memory comprising Data SRAM and Program SRAM, elements 162, 164, Fig. 3, col. 7, lines 41-55). Therefore, in response to applicant's arguments on page 2, paragraphs 3-4 of the Remarks against the Lamb and Rabenko references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument on page 3, first paragraph of the Remarks that there is no suggestion to combine the Lamb and Rabenko references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Lamb discloses a

general network adaptor comprising a voice processor core with MAC circuits while Rabenko discloses a network gateway for processing and transporting voice over IP network for use in a DOCSIS system (col. 12, lines 5-22, Figs. 2 and 3). Rabenko may disclose an exemplary network environment in which the network gateway is involved, which is a DOCSIS environment. However, Rabenko also discloses the internal structure of the network gateway that comprises 802.3 MACs 134 separately coupled to voice and data processor core 160 on a single chip device. Therefore, the network adaptor and the network gateway are analogous and compatible and could be used in the same network environment. The motivation to do so is to provide a highly integrated solution implemented single chip that is compliant with the Data Over Cable Service Interface Specification (DOCSIS) such that the cable modem equipment built by a variety of manufacturers is compatible, which can be found in col. 7, lines 41-48 of Rabenko. In addition, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's argument on page 4, first paragraph of the Remarks that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include

knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Mew whose telephone number is 571-272-3141. The examiner can normally be reached on 9:00 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER 7/30/07